FPGA Implementation of Impulse Synthesis for Radar Receiver using Digital Down Converter

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***Abstract*:**

The impulse synthesis is the method in which the target information is extracted by using digital down converter. DDC is the main processing part of the digital receiver in any RADAR system. The impulse synthesis method using Digital Down Converter (DDC) is discussed in this paper. Xilinx ISE 13.2 software is chosen to design each module of DDC. Then ISim 13.2 functional simulation is used to verify the functionality correctness of the design. The FPGA implemented result is compared with the simulated result of Matlab.

Keywords: Digital Down Converter (DDC), Block RAM, Direct digital synthesizer (DDS), Mixer, Low Pass Filter (LPF), ADC FPGA.

I. INTRODUCTION

In the radar and communication system, receiver is the key component, and its performance will directly affect the whole system operation. Digital radar receiver is a programmable receiver whose functions are extensively defined in software, thus supporting multi-standard or multi-band receiver communications [1]. The Digital radar receiver consists of analog front-end, A/D converter, DDC and digital signal processing processor. Digital Down Converter (DDC) is one of the key technology in the field of radar receivers. It is located between the A/D converter and DSP processor. DDC consists of digital mixer, a digital filtering part. As the FPGA device's performance growing stronger and the costs reducing, it is practical and efficient to design impulse synthesis using DDC based on FPGA.

II.IMPULSE SYNTHESIS BASED DDC

Impulse synthesis is the method in which the target information is extracted in the form of impulses. DDC is the main processing part in this synthesis. The DDC model is based on orthogonal mixing. Sampling data of ADC is mixed with a pair of output sequences of NCO respectively, and the two sequences have the same frequency and $\pi/2$ phase difference [2]. So the digital mixer generates output signal with the sum and difference frequency components. Changing the frequency control words allows NCO output frequency to be modulated. The output signal from digital mixer section will be transmitted to the FIR Low Pass filter. The function of digital filtering is to suppress sum frequency signal due to frequency mixing and the noise residing in aliasing bands [3]. The system architecture with DDC model is shown in figure 1.

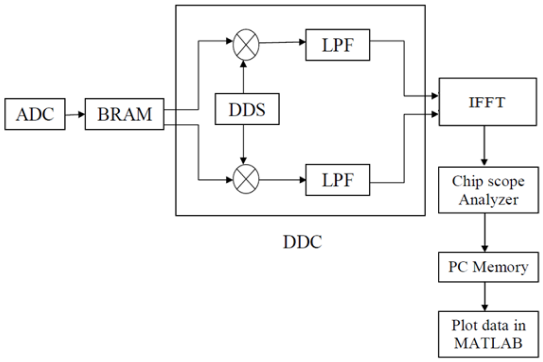

Figure 1: System Architecture

III. FPGA DESIGN OF DDC

The design is realized by Xilinx IP CORE. IP cores are carefully tested and optimized for highest performance in Xilinx's FPGA such as BRAM, DDS, multiplier, FIR filter and FFT IP Core. Use of IP cores reduces the development period as designers can instantiate parameterized blocks of IP quickly, enabling them to concentrate on higher-level design elements and focus on product improvement.

A Digital mixer section

Direct digital synthesizers (DDS), or numerically controlled oscillators (NCO), are important components in many digital communication systems [4]. NCO is aimed to generate sin and cosine waveform in a desired output frequency as shown in the equation :

$s(n) = \sin(\omega_c n) = \sin(2\pi n f_{out} / f_{clk})$. Where f_{out} is the NCO output frequency, f_{clk} is the system clock frequency which is equivalent to the sampling

frequency of input signal used in digital orthogonal mixing. We use the DDS IP CORE to generate digitalized sine and cosine signal as local Oscillator. In this design the system clock is 125MHz, to generate an output sinusoid with frequency *fout* =10.7MHz, the required phase increment is:

$$\Delta\theta = \frac{f_{clk} * 2^{B_{\theta(n)}}}{f_{out}} \quad (1)$$

$$= \frac{10.7 * 2^{16}}{125}$$

$$= 5609_{(10)}$$

The output width $B_{\theta(n)}$ is 16 bits.

Configure the Complex Multiplier IP Core. The cosine [15:0] and sine [15:0] generated by DDS IP Core is set as the real and imaginary components of channel. The Multiplier is treated as a mixer that is combining two input signals. The width of the output is 32 bits. The output of the core is therefore a complex signal. And it's real and imaginary components are named as I and Q. Fig.2 (a) shows the simulation values of cosine and sine components. Fig 2(b) and 2(c) shows the waveform of cosine and sine components.

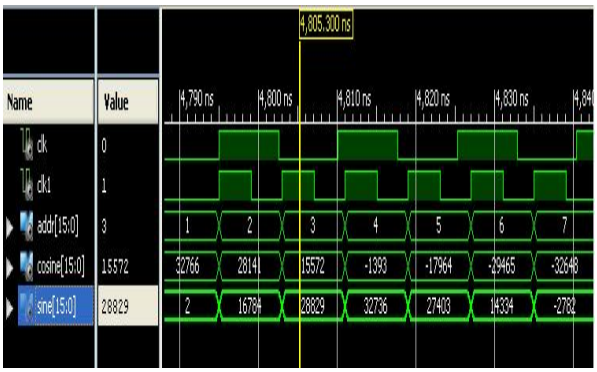

Fig 2(a): simulation of sine and cosine

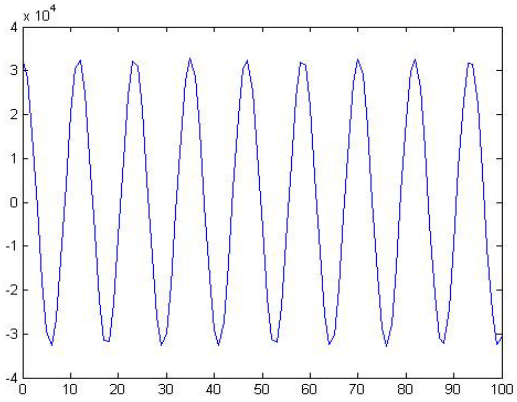

Fig 2(b): cosine waveform

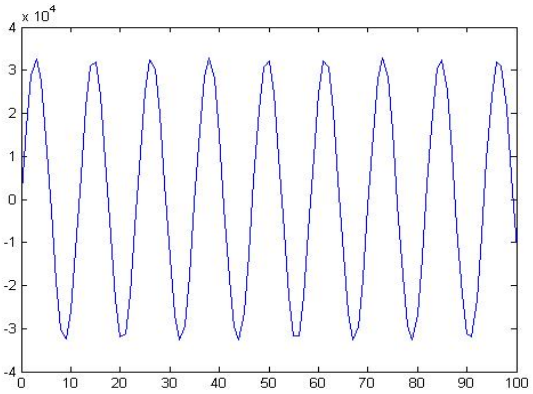

Fig 2(c): sine waveform

B. FIR Low Pass Filter

The FIR low pass filter accepts input samples from the mixer output at the A/D sampling frequency *fs*. Filter Design and Analysis tool is used to implement an FIR (Finite Impulse Response) filter. The filter passes all signals from 0 Hz up to cutoff frequency and rejects all signals above that cutoff frequency. Now, at the filter output we have effectively selected a narrow slice of the RF input signal and translated it to baseband. Note that we have blocked all other signals above and below the band of interest.

A wide range of filter types can be implemented in the Xilinx CORE Generator like single-rate, half-band, Hilbert transform and interpolated filters, in addition to multi-rate filters such as polyphase decimators and interpolators and half-band decimators and interpolators. In this, a single rate FIR filter is implemented. Structure in the coefficient set is exploited to produce area-efficient FPGA implementations [5]. The frequency response of the implemented single rate FIR filter is shown in fig 3. The response is plotted as magnitude verses normalized frequency.

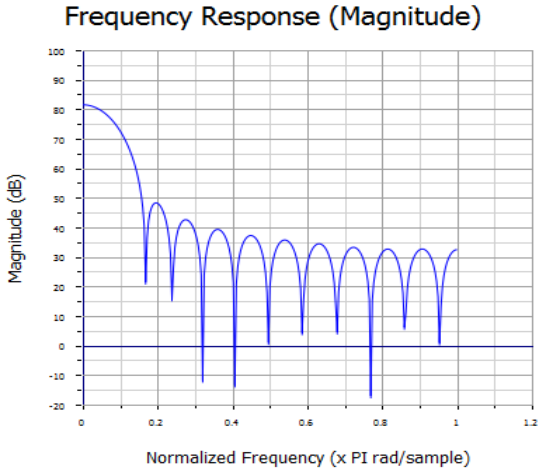

Fig 3: frequency response

The single rate FIR filter is designed by using hamming window with the cut off frequency of 2.5 kHz with the sampling frequency of 125 MHz, The convolution sum defined by this filter is given by the equation (2).

$$y(k) = \sum_{n=0}^{N-1} a(n)x(k-n) \qquad (2)$$

Where k=0, 1, ---

The filtered data is stored in the PC by using Chip scope analyzer. The simulation result of FIR filter is shown in figure 4. The signals li and lq represent the filtered data.

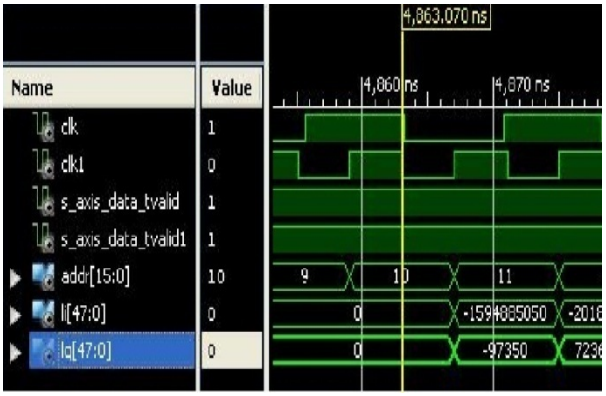

Figure 4: simulation result of filter

IV.SIMULATION RESULTS

The simulation result of MATLAB and FPGA after filtering is shown in fig 5(a) and 5(b) respectively. The IFFT is taken for the filtered I+jQ data. The magnitude of I+jQ data was plotted verses range. The below figures represent the range profiles from MATLAB Simulation and FPGA output.

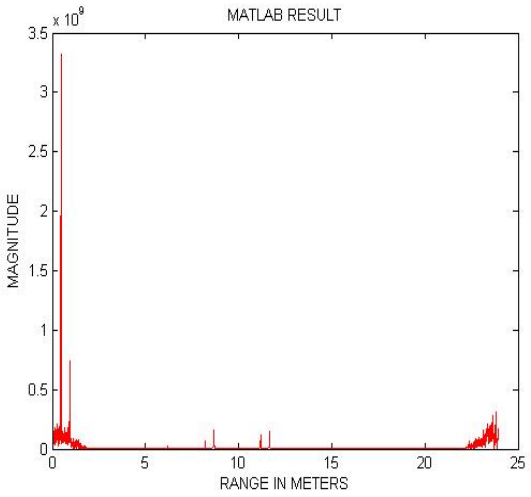

Figure 5(a): MATLAB result

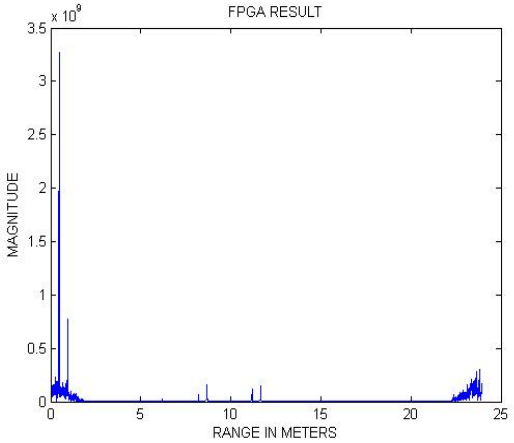

Figure 5(b): FPGA result

Comparing the two results, the FPGA design has the correct function to get the baseband signal. But there are some differences between ideal and actual spectrums. This is because FPGA design has finite word length effect. And the Matlab simulation is double precision floating point operation, so it can approach a better result than the hardware implementation.

V. CONCLUSION

In this paper, we present an FPGA implementation of Impulse synthesis using digital down converter (DDC). The design based on Xilinx IP Core can help to simplify design and reduce development time. Comparing the design result with the ideal result which is generated by Matlab software, it signifies that it has achieved the system requirements that are needed in digital RADAR receivers.

REFERENCES

[1] Yuanbin Wu and Jinwen Li, "The Design of Digital Radar receivers" in the proceedings of "IEEE AES Systems Magazine", January 1998, ISBN: 0885-8985/98, pp: 35-41.

[2] Qingxiang Zhang and Xiaoxiao Su "The Design of Digital Down Converter Based On FPGA" in the proceedings of 8th International conference on WiCOM dated 21-23 sept 2012 IEEE, ISBN: 978-1-61284-683-5, DOI:10.1109/WiCOm.2012.6478707 pp: 1-4.

[3] Panayiotis Savvopoulos and Theodore Antonakopoulos "An IF Digital Down-Converter for Software Radio DVB-S2 Receivers", in the proceedings of 14th IEEE international conference on electronic circuits & systems (ICECS) dated 11-14 Dec 2007 IEEE, ISBN: 1-4244-1378-8, DOI: 10.1109/ICECS.2007.4511172 pp: 1043-1046.

[4] Craig Stringham and David G Long, Brandon Wicks and Glenn Ramsey, "Digital receiver design for an offset IF LFM-CW SAR," in the proceedings of 2011 IEEE, ISBN:978-1-4244-8902-2.

[5] Xilinx inc, LogiCORE IP FIR compiler v5.0 DS534, March 1, 2011.

[6] Xilinx inc, LogiCORE IP DDS compiler v5.0 DS794, March 1, 2011.

[7] A.V Oppenheim and R.W.Schafer, Digital signal proceesing, Englewood, N.J.,Prentice Hall, 3rd Edition 1975.

[8] S.K Mitra, Digital Signal proceesing- A Computer based Approach America:McGraw-Hill Inc,2001.

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